RDK X5 Module

Datasheet

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Revision History

This section tracks the significant documentation changes that occur from release-to-release. The following table lists the technical content changes for each revision.

Revision	Date	Description
0.1	2025-04-30	Initial Draft.

Contents

1 Introduction

1.1 Overview

RDK X5 module equipped with Sunrise 5(X5) chip, which is a highly-integrated, high-performance and power-efficient artificial intelligence System-on-Chip (SoC) powered by D-Robotics.

Based on the Single-core BPU with Bayers-architecture, X5 support real-time pixel-level video segmentation, structured video analysis and attention-based vision perception. The X5 SoC also integrates an Octa-core Cortex A55 CPU, one HiFi5 DSP which can support voice wakeup , an image signal processing (ISP) unit for wide/high dynamic range (WDR or HDR) and noise reduction (3DNR) in the camera input images processing, H.265/H.264/MJPEG video codecs, a 3D GPU supporting OpenGL ES 3.1/3.0 /2.0/1.1.

The RDK X5 module has onboard PMIC and DCDC chips, LPDDR4 and EMMC particles. Its main interfaces include HDMI, Gigabit Ethernet, USB 3.0, MIPI CSI, and MIPI DSI. The module can be optionally equipped with a dual-band 2.4/5GHz wireless module, supports Wi-Fi 6 protocol and Bluetooth 5.4 protocol, and is equipped with a high-performance onboard antenna and supports use with an external antenna kit.

With the advanced toolkit provided by D-Robotics, RDK X5 module can assist customers in rapid mass production.

1.2 Terms and Abbreviations

1.2.1 Terms & Definitions

Terms	Definitions
CSI	Camera Serial Interface
DSI	Display Serial Interface
MIPI	Mobile Industry Processor Interface
SPI	Serial Peripheral Interface
PWM	Pulse Width Modulation
LPWM	Light Pulse Width Modulation

1.2.2 Abbreviations

Abbreviations	Name
BPU	Brain Processing Unit
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output

AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
PU	Pull-Up
PD	Pull-Down
HSIO	High Speed Input/Output
LSIO	Low Speed Input/Output
AON	Always On
RTC	Real Time Clock

1.3 Key Features

- **Extensive Computing Resources**

X5 integrates Octa-core A55 processors, 10Tops BPU, GPU and HiFi5 DSP.

- **Multi-camera inputs**

4×2lane or 2×4lane, up to 2.5Gbps per lane.

ISP Supports 4K@60Hz and maximum resolution of 4096x3072 pixels.

- **Rich Interfaces**

1×USB3.0 HOST, 1×USB2.0 DRD

1×SD, 1×1000M PHY, 1×HDMI

8×UART, 7×I2C, 4×SPI, 4×10bit ADC, 2×I^2S, 2×PDM, 8×PWM, 8×LPWM

Table 1-1 Key Specifications

Modules	Description
CPU	Octa-core Cortex A55, whose typical operating frequency is 1.5GHz L1 cache 32KB, L2 cache 64KB, L3 cache 1MB
BPU	Bayes architecture, up to 10Tops
DSP	HiFi5 Audio DSP@812MHz
GPU	3D GPU, up to 32Gflops 2D GPU, support for multi-surface composition and 2D graphic processing
Memory	32-bit LPDDR4, up to 4266Mbps and 8GB address space. eMMC5.1, support for HS200 SD/SDIO3.0, support for SDR104 QSPI Flash, up to 100MHz
Video Input	MIPI CSI RX

Modules	Description
	Multiple combination modes: 4x2lane or 2x4lane Up to 2.5Gbps per lane Support up to 4 Victual channel
Video Output	Support HDMI, 1080P@60fps Support 4Lane MIPI DSI TX, up to 2560x1440@60fps
ISP	Up to 4K@60fps Maximum resolution of 4096x3072 pixel Support 3D-NR, WDR, HDR, RGB-IR, PDAF
Video Codec	H264/H265, up to 4K@60fps ; MJPEG, up to 16M@30fps
Peripheral	1×USB3.0 HOST, 1×USB2.0 DRD 1×SD, 1×1000M PHY, 1×HDMI 8×UART, 7×I2C, 4×SPI, 4×10bit ADC, 2×I2S, 2×PDM, 8×PWM, 8×LPWM

1.4 Block Diagram

The following figure illustrates the overall design framework of the RDK X5 module.

TBD

Figure 1-1 Functional Block Diagram

2 Interfaces

2.1 Pinout

The RDK X5 module, featuring three independent connectors, offers 260 pinouts. These pinouts carry a diverse range of signals, including those for power supplies, cameras, displays, and Ethernet. In addition, it provides a flexible and extensive set of General-Purpose Input/Output (GPIO) pins. The RDK X5 module supports multiplexing multiple functions on select GPIO pins. For the specific pin definitions and usage guidelines, please refer to *RDK X5 Module Pinout Description and Application Note*.

2.2 Wireless

The RDK X5 module is equipped with an integrated Wi-Fi and Bluetooth communication module, supporting dual-band wireless local area networks in the 2.4/5GHz frequency bands. It adheres to the Wi-Fi 6 protocol and the Bluetooth 5.4 protocol.

Moreover, the module comes with high-performance dual-band onboard antennas and also supports the connection of rod-shaped antennas via the IPEX interface.

The RDK X5 module offers two pins, namely HOST_DIS_WLAN_N_1V8 and HOST_DIS_BT_N_1V8, which are used to switch on/off the Wi-Fi and Bluetooth functions respectively.

By default, the signals of HOST_DIS_WLAN_N_1V8 and HOST_DIS_BT_N_1V8 are pulled high on the module, indicating that the wireless communication is enabled. When these signals are pulled low, the wireless communication modules will be disabled.

2.3 Ethernet

The RDK X5 module is equipped with a Gigabit Ethernet PHY based on MARVELL's 88E1518 chip solution. This is an Integrated 10/100/1000 Mbps Energy-Efficient Ethernet Transceiver.

The PHY supports the Precise Timing Protocol (PTP) Time Stamping, which is based on IEEE 1588 version 2 and IEEE 802.1AS.

The PHY provides two LED control interfaces, namely Ethernet_LED_GREEN_N and Ethernet_LED_YELLOW_N, for driving the status indicator lights on the MagJack. When the module drives these two signals to a low level, the LED indicator lights will illuminate.

MD Pin No.	Signal Name	Description
3	Ethernet_Pair3_P	Ethernet pair 3 positive (connect to transformer or MagJack)
4	Ethernet_Pair1_P	Ethernet pair 1 positive (connect to transformer or MagJack)
5	Ethernet_Pair3_N	Ethernet pair 3 negative (connect to transformer or MagJack)

6	Ethernet_Pair1_N	Ethernet pair 1 negative (connect to transformer or MagJack)
9	Ethernet_Pair2_N	Ethernet pair 2 negative (connect to transformer or MagJack)
10	Ethernet_Pair0_N	Ethernet pair 0 negative (connect to transformer or MagJack)
11	Ethernet_Pair2_P	Ethernet pair 2 positive (connect to transformer or MagJack)
12	Ethernet_Pair0_P	Ethernet pair 0 positive (connect to transformer or MagJack)
15	Ethernet_LED_GREEN_N	Active-low Ethernet speed indicator, typically a green LED is connected to this pin.
17	Ethernet_LED_YELLOW_N	Active-low Ethernet speed indicator, typically a yellow LED is connected to this pin

2.4 USB

The RDK X5 module is equipped with two SoC-integrated USB root ports, specifically a USB 2.0 port and a USB 3.0 port. These ports are directly managed by the SoC's host controller, eliminating the necessity for an intermediate hub conversion.

The USB 3.0 port functions as a device-role SuperSpeed interface. It adheres to the Universal Serial Bus Specification, Revision 3.0, and supports a wide range of speeds, including SuperSpeed (SS), High-Speed (HS), Full-Speed (FS), and Low-Speed (LS).

The USB 2.0 port is designed as a Host/Device dual-role interface. It is compliant with the Universal Serial Bus Specification, Revision 2.0, and supports High-Speed (HS), Full-Speed (FS), and Low-Speed (LS) operations.

By default, the USB 2.0 port operates in the device mode. In this mode, it enables several key functions, such as firmware flashing, debugging, and virtual network card functionality. If there is a requirement to switch the USB 2.0 port to the host mode, the USB2_ID_3V3 pin must be configured to a low-level state.

MD Pin No.	Signal Name	Description
101	USB2_ID_3V3	Input (3.3V signal) USB OTG Pin. Internally pulled up 10K to 3V3. When grounded the Module becomes a USB host but the correct OS driver also needs to be used.
103	USB2_D_N	USB 2.0 D-
105	USB2_D_P	USB 2.0 D+

MD Pin No.	Signal Name	Description
157	USB3_RXN	USB3.0 RX negative

159	USB3_RXP	USB3.0 RX positive
163	USB3_DP	USB3 Port DP
165	USB3_DM	USB3 Port DM
169	USB3_TXN	USB3.0 TX negative
171	USB3_TXP	USB3.0 TX positive

2.5 HDMI

The RDK X5 module provides an HDMI output interface, which supports a resolution of up to 1080P at a frame rate of 60fps.

MD Pin No.	Signal Name	Description
153	HDMI_HPD	Input HDMI hotplug. 5V tolerant. It can be connected directly to a HDMI connector, an ESD protection and a 100k pull down resister need to be designed in the carrier board.
170	HDMI_TX2_P	Output HDMI TX2 positive
172	HDMI_TX2_N	Output HDMI TX2 negative
176	HDMI_TX1_P	Output HDMI TX1 positive
178	HDMI_TX1_N	Output HDMI TX1 negative
182	HDMI_TX0_P	Output HDMI TX0 positive
184	HDMI_TX0_N	Output HDMI TX0 negative
188	HDMI_CLK_P	Output HDMI clock positive
190	HDMI_CLK_N	Output HDMI clock negative
199	HDMI_HSDA	Bidirectional HDMI SDA. Internally pulled up with a 2kΩ. 5V tolerant. It can be connected directly to a HDMI connector, an ESD protection need to be designed in the carrier board.
200	HDMI_HSCL	Bidirectional HDMI SCL. Internally pulled up with a 2kΩ. 5V tolerant. It can be connected directly to a HDMI connector, an ESD protection need to be designed in the carrier board.

2.6 MIPI

RDK X5 module supports for both the MIPI DSI and CSI protocols. In particular, the CSI interface of the RDK X5 module is capable of accommodating up to four independent MIPI links, providing enhanced flexibility and expandability for various applications.

2.6.1 MIPI DSI TX interface

The module is compatible with the MIPI Alliance Interface specification v1.2, supporting 1 clock lane and up to 4 data lanes, with a maximum data rate of 2.5 Gbps per lane.

MD Pin No.	Signal Name	MD Pin No.	Signal Name
175	DSI_D0_N	189	DSI_C_P
177	DSI_D0_P	193	DSI_D2_N
181	DSI_D1_N	194	DSI_D3_N
183	DSI_D1_P	195	DSI_D2_P
187	DSI_C_N	196	DSI_D3_P

2.6.2 MIPI CSI RX interface

The module is compatible with the MIPI Alliance Interface Specification DPHY V2.1. It supports up to 8 data lanes, with a maximum data rate of 2.5 Gbps per lane.

The CSI interface supports up to 4 MIPI RX links. In this case, each link has an independent differential clock and two data links. Additionally, the CSI interface supports combining 2-lane CSI configurations into a 4-lane CSI application.

MD Pin No.	Signal Name	MD Pin No.	Signal Name
127	CSI0_CLK_N	140	CSI2_CLK_N
129	CSI0_CLK_P	142	CSI2_CLK_P
115	CSI0_D0_N	128	CSI2_D0_N
117	CSI0_D0_P	130	CSI2_D0_P
121	CSI0_D1_N	134	CSI2_D1_N
123	CSI0_D1_P	136	CSI2_D1_P
152	CSI1_CLK_N	164	CSI3_CLK_N
154	CSI1_CLK_P	166	CSI3_CLK_P
133	CSI1_D0_N	118	CSI3_D0_N
135	CSI1_D0_P	116	CSI3_D0_P
139	CSI1_D1_N	124	CSI3_D1_N
141	CSI1_D1_P	122	CSI3_D1_P

The RDK X5 Module provides a rich set of GPIO outputs. When working with the default software driver, CAM1_EN_1V8 and CAM2_EN_1V8 are used for the enable and reset control of camera modules, adopting 1.8V digital logic. AON_GPIO1_3V3 is employed for the enable control of cameras with 3.3V digital logic.

For the default configuration of the camera I2C in software, please refer to the I2C section of this document.

2.7 SD

The RDK X5 Module provides a single SD 3.0 host controller, which utilizes four-wire communication. It supports SDR12 at 25 MHz, SDR25 at 50 MHz, SDR50 at 100 MHz, and SDR104 at 200 MHz, and is capable of adaptively supporting the two voltage level standards of 3.3V and 1.8V for SD cards.

The module offers a control pin named TF_VDD33_RST_3V3 for SD card power supply, which is used to reset the SD card. In the case of using a core module without an on-board EMMC, the SD card will serve as the boot medium. In the design of the carrier board, this control pin must be set to a high level by default. It is recommended to pull it up to 3.3V through a 10k resistor.

The module provides an SD card insertion detection signal named SDIO_TF_CD_ADJ. When a TF card is inserted, this pin should be at a high level.

MD Pin No.	Signal Name	Description
57	SDIO_TF_SCLK_ADJ	SD card clock signal
61	SDIO_TF_DAT3_ADJ	SD card Data3 signal
62	SDIO_TF_CMD_ADJ	SD card Command signal
63	SDIO_TF_DAT0_ADJ	SD card Data0 signal
67	SDIO_TF_DAT1_ADJ	SD card Data1 signal
69	SDIO_TF_DAT2_ADJ	SD card Data2 signal
75	TF_VDD33_RST_3V3	Output to power-switch for the SD card. The module sets this pin high (3.3V) to signal that power to the SD card should be turned on.
258	SDIO_TF_CD_ADJ	GPIO: Card Detect signal, internally pulled up 47K to power. When TF inserted, this pin should be high.

2.8 Low Speed Interface

2.8.1 I2S

The RDK X5 Module provides two I2S interfaces, both of which are full-duplex interfaces and support a maximum data rate of 40 Mbps in master mode. Specifically, in RX mode, it supports 1/2/4/8/16-channel audio input, and in TX mode, it supports 1/2-channel audio output.

I2S0 operates with a 1.8V logic level, while I2S1 supports the switching between two voltage levels of 1.8V and 3.3V.

MD Pin No.	Signal Name	Description
236	CODEC_I2S0_DO_1V8	GPIO: typically a 1.8V signal, Data Output line for the I2S0
238	CODEC_I2S0_SCLK_1V8	GPIO: typically a 1.8V signal, MCLK signal for the I2S0

240	CODEC_I2S0_WS_1V8	GPIO: typically a 1.8V signal, Word Select signal for the I2S0
242	CODEC_I2S0_DI_1V8	GPIO: typically a 1.8V signal, Data Input line for the I2S0
246	CODEC_I2S0_MCLK_1V8	GPIO: typically a 1.8V signal, Master Clock (MCLK) signal for the I2S0

MD Pin No.	Signal Name	Description
25	HIFI_I2S1_DO_VREF	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
26	HIFI_I2S1_WS_VREF	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
27	HIFI_I2S1_DI_VREF	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
49	HIFI_I2S1_SCLK_VREF	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
54	HIFI_I2S1_MCLK_VREF	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V

2.8.2 PDM

The RDK X5 Module provides two PDM interfaces, which can meet the input requirements of digital microphones. On the module, these functions are multiplexed with other GPIO functions and need to be switched through software configuration.

MD Pin No.	Signal Name	Description
21	LED_SYS_STATUS_1V8	Pin Function Multiplex: - HIFI_PDM_CKO
89	HOST_DIS_WLAN_N_1V8	Pin Function Multiplex: - HIFI_PDM_IN1
91	HOST_DIS_BT_N_1V8	Pin Function Multiplex: - HIFI_PDM_IN0

2.8.3 SPI

The RDK X5 Module offers up to four SPI interfaces. Among them, SPI1 supports two chip-select signals. The SPI interfaces support both master mode and slave mode. In master mode, the maximum data rate is 50 Mbps, and in slave mode, the maximum data rate is 32 Mbps.

MD Pin No.	Signal Name	Description

37	LSIO_SPI1_SSN0_JTAG_TRSTN_VREF	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
38	LSIO_SPI1_SCLK_JTAG_TCK_VREF	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
39	LSIO_SPI1_SSN1_JTAG_TMS_VREF	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
40	LSIO_SPI1_MISO_JTAG_TDI_VREF	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
44	LSIO_SPI1_MOSI_JTAG_TDO_VREF	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V

MD Pin No.	Signal Name	Description
24	LSIO_SPI2_MISO_PWM2_VREF	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
30	LSIO_SPI2_CS_PWM1_VREF	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
34	LSIO_SPI2_SCLK_PWM0_VREF	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
45	LSIO_SPI2_MOSI_PWM3_VREF	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V

MD Pin No.	Signal Name	Description
70	CAM1_MCLK_1V8	Pin Function Multiplex： - MCLK - LPWM - SPI3_SCLK
72	CAM2_MCLK_1V8	Pin Function Multiplex： - MCLK - LPWM - SPI3_SSN
237	CAM3_MCLK_1V8	Pin Function Multiplex： - MCLK - LPWM - SPI3_MISO
239	CAM4_MCLK_1V8	Pin Function Multiplex： - MCLK - LPWM - SPI3_MOSI

MD Pin No.	Signal Name	Description

203	CAN_SPI5_MISO	GPIO: Typically a 1.8V signal, SPI5 Master In Slave Out, default for CAN controllers and transceivers in the RDK X5.
204	CAN_SPI5_CS	GPIO: Typically a 1.8V signal, SPI5 Chip Select, default for CAN controllers and transceivers in the RDK X5.
205	CAN_SPI5_MOSI	GPIO: Typically a 1.8V signal, SPI5 Master Out Slave In, default for CAN controllers and transceivers in the RDK X5.
206	CAN_SPI5_SCLK	GPIO: Typically a 1.8V signal, SPI5 Serial Clock, default for CAN controllers and transceivers in the RDK X5.

2.8.4 I2C

The RDK X5 Module supports 7 I2C interfaces. Only I2C4 supports a data rate of 3.4 Mbps, while I2C0, I2C1, I2C2, I2C3, I2C5, and I2C6 only support up to 400 KHz and the SMBus protocol. Among them, I2C2 is a dedicated interface for the platform's PMIC and is not used as an interface for peripheral devices.

When paired with the default software driver, I2C2 and I2C6 are utilized as the I2C control buses for two cameras, employing 1.8V digital logic. I2C3 serves as the camera I2C bus with 3.3V digital logic.

MD Pin No.	Signal Name	Description
35	LSIO_SCL0_PWM4_VREF	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V. Internal 2kΩ pull up to GPIO_VREF
36	LSIO_SDA0_PWM5_VREF	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V. Internal 2kΩ pull up to GPIO_VREF

MD Pin No.	Signal Name	Description
28	LSIO_SDA1_PWM7_VREF	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V. Internal 2kΩ pull up to GPIO_VREF
31	LSIO_ SCL1_PWM6_VREF	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V. Internal 2kΩ pull up to GPIO_VREF

MD Pin No.	Signal Name	Description
80	LSIO_SCL3_3V3	I2C clock pin, may be used for Camera and Display. Internal 4kΩ pull up to MD_3.3V
82	LSIO_SDA3_3V3	I2C Data pin, may be used for Camera and Display. Internal 4kΩ pull up to MD_3.3V

MD Pin No.	Signal Name	Description
225	CAM2_SDA4_1V8	GPIO: typically a 1.8V signal, Camera2 Serial Data Line in RDK X5, no pull up resisters in the module.
227	CAM2_SCL4_1V8	GPIO: typically a 1.8V signal, Camera2 Serial Clock Line in RDK X5, no pull up resisters in the module.

MD Pin No.	Signal Name	Description
56	LSIO_SCL5_RX3_VREF	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V. Internal 4kΩ pull up to GPIO_VREF
58	LSIO_SDA5_TX3_VREF	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V. Internal 4kΩ pull up to GPIO_VREF

MD Pin No.	Signal Name	Description
241	CAM1_SDA6_1V8	GPIO: typically a 1.8V signal, Camera1 Serial Data Line in RDK X5, no pull up resisters in the module.
243	CAM1_SCL6_1V8	GPIO: typically a 1.8V signal, Camera1 Serial Clock Line in RDK X5, no pull up resisters in the module.

MD Pin No.	Signal Name	Description
209	CODEC_HDMI_SCL7	GPIO: Typically a 1.8V signal, Serial Clock Line, the clock signal for the I2C bus. By default, it is used as I2C for codec (located on the carrier board) and HDMI converter chip (located on the module) in the RDK X5.
211	CODEC_HDMI_SDA7	GPIO: Typically a 1.8V signal, Serial Data Line, the data line for the I2C bus

2.8.5 UART

The RDK X5 Module provides 8 UART interfaces. Among them, UART0 is a dedicated interface for system debugging and operates at a frequency of 921600 bps.

UART2, UART3, UART4, UART5, UART6, and UART7 support baud rates of 9600, 38400, 57600, 921600, 115200, and 4M.

UART2, UART3, UART4, UART5, and UART6 support the standard mode.

UART7 supports the auto-flow control mode.

UART5 is used for the onboard Bluetooth and WiFi modules and cannot be used for other peripherals.

MD Pin No.	Signal Name	Description

64	DEBUG_UART0_TXD_1V8	Uart Data TX pin, a 1.8V signal, used to debug X5 chip
68	DEBUG_UART0_RXD_1V8	Uart Data RX pin, a 1.8V signal, used to debug X5 chip

MD Pin No.	Signal Name	Description
51	LSIO_UART1_RX_VREF	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
55	LSIO_UART1_TX_VREF	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V

MD Pin No.	Signal Name	Description
41	LSIO_UART2_RX_VREF	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
46	LSIO_UART2_TX_VREF	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V

MD Pin No.	Signal Name	Description
56	LSIO_SCL5_RX3_VREF	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V. Internal 1.8kΩ pull up to GPIO_VREF
58	LSIO_SDA5_TX3_VREF	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V. Internal 1.8kΩ pull up to GPIO_VREF

MD Pin No.	Signal Name	Description
215	UART4_RXD	GPIO: Receive Data line for UART4, typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
217	UART4_TXD	GPIO: Transmit Data line for UART4, typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V

MD Pin No.	Signal Name	Description
29	LSIO_UART7_CTS_N_VREF	Pin Function Multiplex：UART6_RX
47	LSIO_UART7_RTS_N_VREF	Pin Function Multiplex：UART6_TX

MD Pin No.	Signal Name	Description
29	LSIO_UART7_CTS_N_VREF	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
47	LSIO_UART7_RTS_N_VREF	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V

48	LSIO_UART7_RX_VREF	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
50	LSIO_UART7_TX_VREF	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V

2.8.6 PWM

The RDK X5 Module supports 8 PWM interfaces. The frequency of the output waveform is programmable, ranging from 0.05 Hz to 1MHz. It also provides a reference mode and can output waveforms with various duty cycles.

MD Pin No.	Signal Name	Description
34	LSIO_SPI2_SCLK_PWM0_VREF	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
30	LSIO_SPI2_CS_PWM1_VREF	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
24	LSIO_SPI2_MISO_PWM2_VREF	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
45	LSIO_SPI2_MOSI_PWM3_VREF	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
35	LSIO_SCL0_PWM4_VREF	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V. Internal 2kΩ pull up to GPIO_VREF
36	LSIO_SDA0_PWM5_VREF	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V. Internal 2kΩ pull up to GPIO_VREF
31	LSIO_ SCL1_PWM6_VREF	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V. Internal 2kΩ pull up to GPIO_VREF
28	LSIO_SDA1_PWM7_VREF	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V. Internal 2kΩ pull up to GPIO_VREF

2.8.7 LPWM

RDK X5 Module provides a total of 8 channels of LPWM.

- The frequency of the output pulse is programmable, ranging from 1 Hz to 1 MHz.
- The width of the output pulse is programmable, ranging from 1 μs to 4 ms.
- It supports generating output pulses with multiple trigger sources, such as PPS, EMAC, and the internal system timer.

The four channels of signals (Pin 70, Pin 72, Pin 237, Pin 239) are based on the same clock source. Therefore, when used for LPWM synchronization, they can be directly connected one-to-one without the need for a one-to-many connection method.

The four channels of signals (Pin 203, Pin 204, Pin 205, Pin 206) are based on the same clock source.

MD Pin No.	Signal Name	Description
206	CAN_SPI5_SCLK	Pin Function Multiplex：LPWM0
204	CAN_SPI5_CS	Pin Function Multiplex：LPWM1
203	CAN_SPI5_MISO	Pin Function Multiplex：LPWM2
205	CAN_SPI5_MOSI	Pin Function Multiplex：LPWM3
70	CAM1_MCLK_1V8	Pin Function Multiplex：LPWM4
72	CAM2_MCLK_1V8	Pin Function Multiplex：LPWM5
237	CAM3_MCLK_1V8	Pin Function Multiplex：LPWM6
239	CAM4_MCLK_1V8	Pin Function Multiplex：LPWM7

2.8.8 MCLK

The RDK X5 Module provides four channels of MCLK signals, which can be used to drive the camera module.

MD Pin No.	Signal Name	Description
70	CAM1_MCLK_1V8	Pin Function Multiplex：LPWM4
72	CAM2_MCLK_1V8	Pin Function Multiplex：LPWM5
237	CAM3_MCLK_1V8	Pin Function Multiplex：LPWM6
239	CAM4_MCLK_1V8	Pin Function Multiplex：LPWM7

2.9 ADC

The RDK X5 Module has 4 ADCs. Among them, ADC7 is used for the hardware identification of the carrier board, which facilitates customers to distinguish the board ID. The other 3 ADCs can be used for various types of data collection and voltage monitoring.

MD Pin No.	Signal Name	Description
210	ADC_VINS4	The 4th ADC input channel, maximum input voltage of 1.8V
212	ADC_VINS3	The 3rd ADC input channel, maximum input voltage of 1.8V
216	ADC_VINS7_RSVD	The 7th ADC input channel, maximum input voltage of 1.8V.
218	ADC_VINS5	The 5th ADC input channel, maximum input voltage of 1.8V

2.10 AON GPIO

The RDK X5 Module supports the sleep mode. The following three GPIOs can wake up the X5 in sleep mode. Among them, AON_FLASH_SLEEP_RESUME_N_1V8 is fixedly used for the sleep/wake-up function in the software. AON_GPIO0 and AON_GPIO4 has a 10k pull-up resistor design, and the pull-up voltage level is 1.8V on the module and can be further developed on the baseboard according to requirements.

When using the sleep-wakeup function, if the X5 chip is in sleep mode, the peripherals need to be

powered to ensure that the peripherals can generate valid interrupt signals.

MD Pin No.	Signal Name	Description
222	AON_GPIO4	GPIO: typically a 1.8V signal, can be used for interrupt wakeup in sleep mode
248	AON_GPIO0	GPIO: typically a 1.8V signal, can be used for interrupt wakeup in sleep mode
93	AON_FLASH_SLEEP_RESUME_N_1V8	Low level on this pin realizes different function. This pin is not connected to any net on the module. By pulling it low, the X5 minimum system can be switched between sleep and wake-up states. Pull it low during the system startup phase to perform the burning operation.

2.11 Indicator Lights

The RDK X5 Module provides two indicator light control interfaces. Both interfaces are only for on-off control and cannot be used as the anode or cathode of an LED for driving or sinking functions. If MD_LED_PWR_N_1V8 is not used to indicate the power-on completion status, leave it floating. It cannot be used for other functions.

MD Pin No.	Signal Name	Description
21	LED_SYS_STATUS_1V8	GPIO: typically a 1.8V signal. By default, active-high output to drive Power On LED in the carrier board, which indicates that the running status of software.
95	MD_LED_PWR_N_1V8	Active-low output to drive Power On LED in the carrier board, which indicates that the X5 minimum system power-up is complete and reset is released.

2.12 System Control

The RDK X5 Module provides the following pins for system control-related purposes.

MD Pin No.	Signal Name	Description
78	GPIO_VREF	Must be connected to MD_3.3V (pins 84 and 86) for 3.3V GPIO or MD_1.8V (pins 88 and 90) for 1.8V GPIO.
89	HOST_DIS_WLAN_N_1V8	GPIO: Can be left floating; if driven low the wireless interface will be disabled. Internally pulled up via 10kΩ to 1.8V
91	HOST_DIS_BT_N_1V8	GPIO: Can be left floating; if driven low the Bluetooth interface will be disabled. Internally pulled up via 10kΩ to 1.8V

92	SYS_HW_RESET_N_1V8	Can be left floating; if driven low the system will be reset. Internally pulled up via 100kΩ to 1.8V
93	AON_FLASH_SLEEP_RESUME_N_1V8	Low level on this pin realizes different function. This pin is not connected to any net on the module. By pulling it low, the X5 minimum system can be switched between sleep and wake-up states. Pull it low during the system startup phase to perform the burning operation.
99	GLOBAL_EN	Input. Drive low to power off Module. Internally pulled up with a 10kΩ to +5V
100	RESETN_OUT_3V3	Output. An active-low reset output signal and generated by X5 module. The reset signal will be output in the following scenarios: hardware reset, software reset, watchdog timeout and entering sleep mode.
216	ADC_VINS7_RSVD	The 7th ADC input channel, maximum input voltage of 1.8V. Reserved, this ADC is used for carrier board version identification.

3 Power

3.1 Power Consumption

It is recommended to supply power to the RDK X5 Module with a minimum of 3A at 5V to ensure the stable operation of the module under maximum load. The module is designed with a total of 11 VDD_5V_IN input power pins to supply power to the core module.

It should be noted that the core board has a clear voltage range requirement for the 5V supply.

- The over-voltage lockout (OVLO) protection voltage is 5.25V
- The minimum operating voltage is 4.75V.

3.2 Module Output Power

The RDK X5 Module has two output power supply pins, namely VDDIO18_DSP_UART, MD_3.3V and MD_1.8V.

- VDDIO18_DSP_UART: The output voltage of this pin is only used to pull up the system debug serial port DEBUG_UART0 (Pin64, Pin68). It is strictly forbidden to use it for any other load. If there is no need, please keep it floating.
- MD_3.3V and MD_1.8V: These two voltage levels are typically used to select GPIO_VREF on the carrier board and enable related power ICs and for I2C pull-up. It is not recommended to drive the load directly.
- If there is a power supply requirement for driving peripherals on the carrier board, the best approach is to configure a separate power supply chip.

3.3 RTC Power

The RDK X5 Module supports the RTC (Real Time Clock) function, which is implemented based on the on-board PMIC. The power pin of this function is VRTC (Pin76), and the requirements are as follows.

- When the external RTC battery is powering the system, the battery voltage is required to be 2~3.3V, and its current discharge capacity should be greater than 2.5uA.
- When the PMIC charges the RTC, the maximum charging voltage that the selected RTC battery can withstand is required to be no less than 3.3V, and the maximum allowable charging current is required to be no less than 1mA.
- When the module is powered only by the RTC battery, it only supports counting and clock functions, and cannot wake up the X5 with an alarm.

3.4 GPIO VREF

The RDK X5 module has 29 GPIOs with switchable voltage domains, which can support both 3.3V and 1.8V. These GPIOs implement level logic switching according to the different voltages of the GPIO_VREF (Pin78).

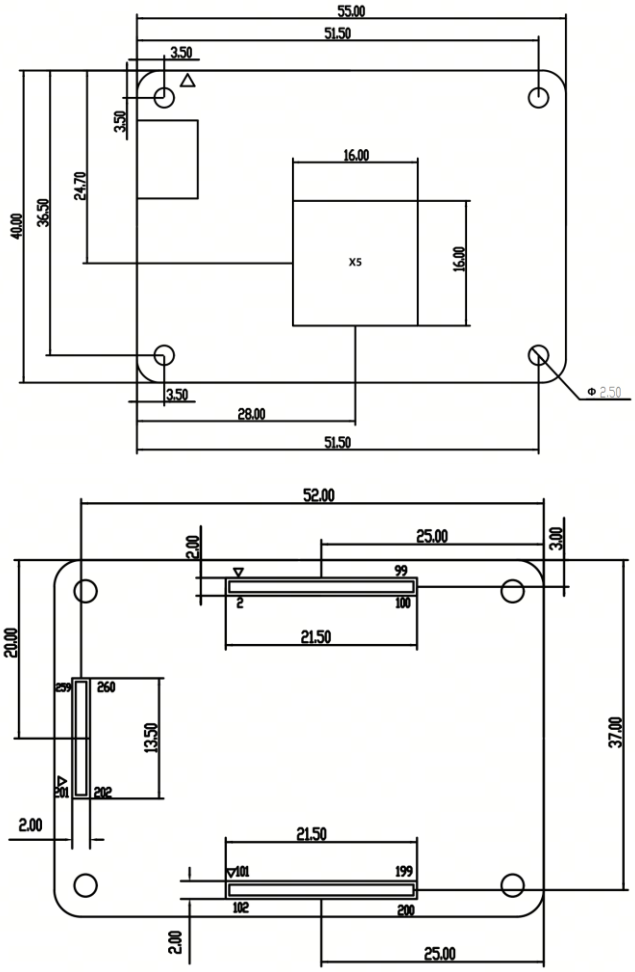
- GPIO_VREF must be connected to MD_3.3V (pins 84 and 86) for 3.3V GPIO.

- GPIO_VREF must be connected to MD_1.8V (pins 88 and 90) for 1.8V GPIO.

4 Mechanical

4.1 Module

As shown in the figure below, these are the key structural dimensions of the RDK X5 module.



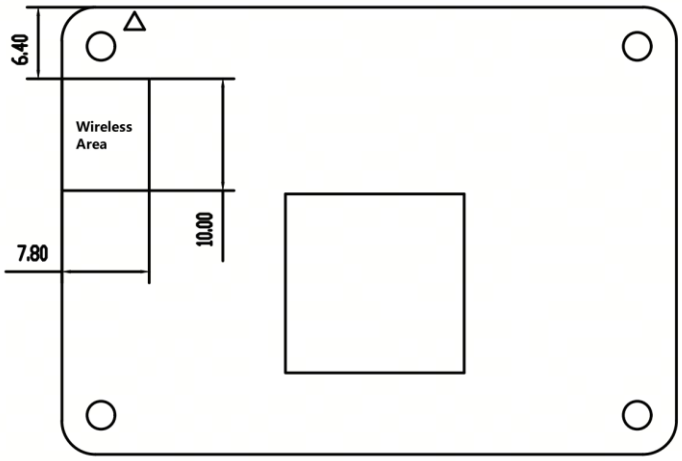
4.2 Connector

The entire board of the RDK X5 Module is equipped with three connectors, which come in two specifications. Except for the total number of pins, the parameters of the other connectors are the same.

Package	Pitch	Number of Rows	Current Rating
SMD	0.4mm	2	300mA

4.3 Wireless Cutout

The RDK X5 module supports onboard WiFi antenna modules, so in the carrier board design, clearance design should be done at the corresponding projection position.



5 Order

Part Number	Wireless	RAM	eMMC
RDKX5MD002000	No	2GB	N/A
RDKX5MD002016			16GB
RDKX5MD002032			32GB
RDKX5MD002064			64GB
RDKX5MD004000		4GB	N/A
RDKX5MD004016			16GB
RDKX5MD004032			32GB
RDKX5MD004064			64GB
RDKX5MD008000		8GB	N/A
RDKX5MD008016			16GB
RDKX5MD008032			32GB
RDKX5MD008064			64GB
RDKX5MD102000	Yes	2GB	N/A
RDKX5MD102016			16GB
RDKX5MD102032			32GB
RDKX5MD102064			64GB
RDKX5MD104000		4GB	N/A
RDKX5MD104016			16GB
RDKX5MD104032			32GB
RDKX5MD104064			64GB
RDKX5MD108000		8GB	N/A
RDKX5MD108016			16GB
RDKX5MD108032			32GB
RDKX5MD108064			64GB