# RDK X5 Module

## Hardware Design Guide

**Rev. 1.0**

**May 2025**

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# Revision History

This section tracks the significant documentation changes that occur from release-to-release. The following table lists the technical content changes for each revision.

| Revision | Date | Description |
|---|---|---|
| 1.0 | 2025-05-26 | Initial release. |
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# Contents

# 1 Introduction

## 1.1 Overview

RDK X5 module equipped with Sunrise 5(X5) chip, which is a highly-integrated, high-performance and power-efficient artificial intelligence System-on-Chip (SoC) powered by D-Robotics.

Based on the Single-core BPU with Bayers-architecture, X5 support real-time pixel-level video segmentation, structured video analysis and attention-based vision perception. The X5 SoC also integrates an Octa-core Cortex A55 CPU, one HiFi5 DSP which can support voice wakeup , an image signal processing (ISP) unit for wide/high dynamic range (WDR or HDR) and noise reduction (3DNR) in the camera input images processing, H.265/H.264/MJPEG video codecs, a 3D GPU supporting OpenGL ES 3.1/3.0 /2.0/1.1.

The RDK X5 module has onboard PMIC and DCDC chips, LPDDR4 and EMMC particles. Its main interfaces include HDMI, Gigabit Ethernet, USB 3.0, MIPI CSI, and MIPI DSI. The module can be optionally equipped with a dual-band 2.4/5GHz wireless module, supports Wi-Fi 6 protocol and Bluetooth 5.4 protocol, and is equipped with a high-performance onboard antenna and supports use with an external antenna kit.

With the advanced toolkit provided by D-Robotics, RDK X5 module can assist customers in rapid mass production.

## 1.2 Terms and Abbreviations

### 1.2.1 Terms & Definitions

| Terms | Definitions |
|---|---|
| CSI | Camera Serial Interface |
| DSI | Display Serial Interface |
| MIPI | Mobile Industry Processor Interface |
| SPI | Serial Peripheral Interface |
| PWM | Pulse Width Modulation |
| LPWM | Light Pulse Width Modulation |

### 1.2.2 Abbreviations

| Abbreviations | Name |
|---|---|
| BPU | Brain Processing Unit |
| DI | Digital Input |
| DO | Digital Output |
| DIO | Digital Input/Output |

| | |
|---|---|
| AI | Analog Input |
| AO | Analog Output |
| AIO | Analog Input/Output |
| PU | Pull-Up |
| PD | Pull-Down |
| HSIO | High Speed Input/Output |
| LSIO | Low Speed Input/Output |
| AON | Always On |
| RTC | Real Time Clock |

## 1.3 References Documents

Refer to the following list of documents or models for more information. Use the latest revision of all documents.

***RDK X5 Module Pinout Description and Application Note***

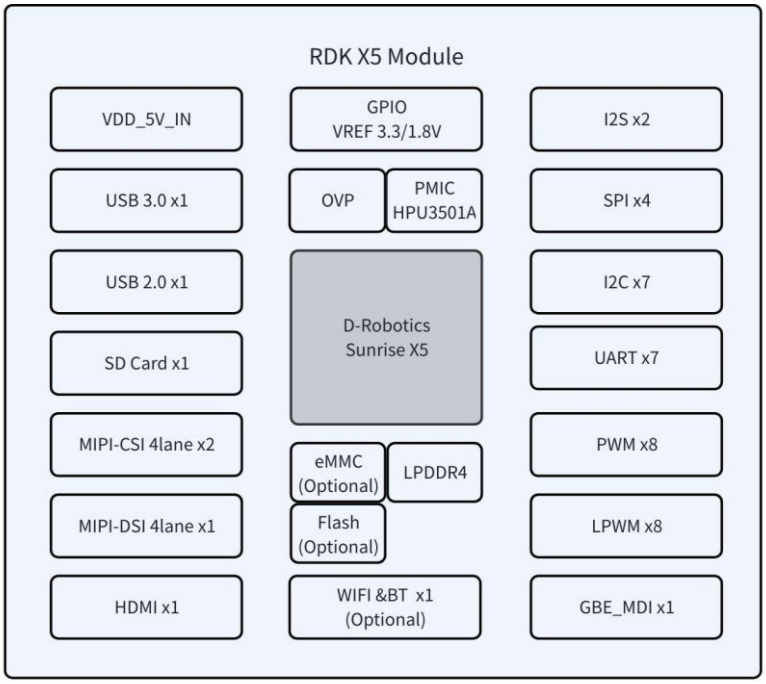
***RDK X5 Module Datasheet***

***RDK X5 Module Carrier Board***

This design guide contains recommendations and guidelines for engineers to follow to create a product that is optimized to achieve the best performance from the interfaces supported by the RDK X5 Module.

## 1.4 Block Diagram

The following figure illustrates the overall design framework of the RDK X5 module.

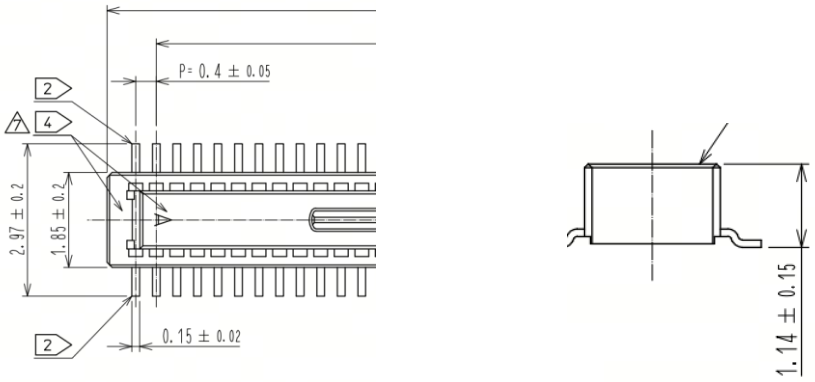


## 1.5 Pinout

The RDK X5 module, featuring three independent connectors, offers 260 pinouts. These pinouts carry a diverse range of signals, including those for power supplies, cameras, displays, and Ethernet. In addition, it provides a flexible and extensive set of General-Purpose Input/Output (GPIO) pins. The RDK X5 module supports multiplexing multiple functions on select GPIO pins. For the specific pin definitions and usage guidelines, please refer to ***RDK X5 Module Pinout Description and Application Note***.

The three connectors has two specifications. Except for the total number of pins, the parameters of the other connectors are the same.

| Package | Pitch | Number of Rows | Current Rating |
|---|---|---|---|
| SMD | 0.4mm | 2 | 300mA |



# 2 Hardware Design Recommendation

## 2.1 Power

### 2.1.1 Power Consumption

RDK X5 Module has integrated PMIC and DCDC chips, so only need supply a 5V power through VDD_5V_IN pin to power up the Module.

- It is recommended to supply power to the RDK X5 Module with a minimum of 3A at 5V to ensure the stable operation of the module under maximum load.
- The module is designed with a total of 11 VDD_5V_IN input power pins to supply power to the core module.

| MD Pin No. | Signal Name | Description |
|---|---|---|
| 77,79,81,83,85,87,249.251,253, 255,257 | VDD_5V_IN (Input) | 4.75V-5.25V. Main power input. Power input max 300mA per pin. RDK X5 MD requires at least 3A@5V. |

***NOTE:***

It should be noted that the core board has a clear voltage range requirement for the 5V supply.

1. The over-voltage lockout (OVLO) protection voltage is 5.25V
2. The minimum operating voltage is 4.75V.

### 2.1.2 Module Output Power

The RDK X5 Module has two output power supply pins, namely VDDIO18_DSP_UART, MD_3.3V and MD_1.8V.

- VDDIO18_DSP_UART (Pin231): The output voltage of this pin is only used to pull up the system debug serial port DEBUG_UART0 (Pin64, Pin68). It is strictly forbidden to use it for any other load. If there is no need, please keep it floating.
- MD_3.3V and MD_1.8V: These two voltage levels are typically used to select GPIO_VREF on the carrier board and enable related power ICs and for I2C pull-up. It is not recommended to drive the load directly.
- If there is a power supply requirement for driving peripherals on the carrier board, the best approach is to configure a separate power supply chip.

### 2.1.3 GPIO VREF

The RDK X5 module has 29 GPIOs with switchable voltage domains, which can support both 3.3V and 1.8V. These GPIOs implement level logic switching according to the different voltages of the GPIO_VREF (Pin78).

- GPIO_VREF must be connected to MD_3.3V (pins 84 and 86) for 3.3V GPIO.

- GPIO_VREF must be connected to MD_1.8V (pins 88 and 90) for 1.8V GPIO.
- GPIO_VREF cannot be floating, otherwise the system will not work properly.

### 2.1.4 Peripherals Power

It is usually necessary to provide 5V, 3.3V, and 1.8V power to peripherals. It is necessary to ensure that these power supplies are powered up later than the system power supply. It is recommended to use MD_3.3V and MD_1.8V as the enable of peripheral power supply.

### 2.1.5 RTC Power

The RDK X5 Module supports the RTC (Real Time Clock) function, which is implemented based on the on-board PMIC. The power pin of this function is VRTC (Pin76), and the requirements are as follows.

- When the external RTC battery is powering the system, the battery voltage is required to be 2~3.3V, and its current discharge capacity should be greater than 2.5uA. The VRTC(Pin76) is connected in series with a 4.7KΩ resistor on the module for current limiting.
- When the PMIC charges the RTC, the maximum charging voltage that the selected RTC battery can withstand is required to be no less than 3.3V, and the maximum allowable charging current is required to be no less than 1mA.
- When the module is powered only by the RTC battery, it only supports counting and clock functions, and cannot wake up the X5 with an alarm.

## 2.2 System Control

The RDK X5 Module provides the following pins for system control-related purposes.

| MD Pin No. | Signal Name | Description |
|---|---|---|
| 160 | EMMC_BOOT | System startup control pin. Internally pulled up via 100kΩ to 1.8V. If the system is started from eMMC, pull this pin down to ground through a 4.7K resistor at carrier board. By default, this pin is left floating and the system boots from NAND Flash. |
| 78 | GPIO_VREF | Must be connected to MD_3.3V (pins 84 and 86) for 3.3V GPIO or MD_1.8V (pins 88 and 90) for 1.8V GPIO. |
| 89 | HOST_DIS_WLAN_N_1V8 | GPIO: Can be left floating; if driven low the wireless interface will be disabled. Internally pulled up via 10kΩ to 1.8V |
| 91 | HOST_DIS_BT_N_1V8 | GPIO: Can be left floating; if driven low the Bluetooth interface will be disabled. Internally pulled up via 10kΩ to 1.8V |

| | | |
|---|---|---|
| 92 | SYS_HW_RESET_N_1V8 | Can be left floating; if driven low the system will be reset. Internally pulled up via 100kΩ to 1.8V |
| 93 | AON_FLASH_SLEEP_RESUME_N_1V8 | Low level on this pin realizes different function. This pin is not connected to any net on the module. By pulling it low, the X5 minimum system can be switched between sleep and wake-up states. Pull it low during the system startup phase to perform the burning operation. |
| 99 | GLOBAL_EN | Input. Drive low to power off Module. Internally pulled up with a 10kΩ to +5V |
| 100 | RESETN_OUT_3V3 | Output. An active-low reset output signal and generated by X5 module. The reset signal will be output in the following scenarios: hardware reset, software reset, watchdog timeout and entering sleep mode. |
| 216 | ADC_VINS7_RSVD | The 7th ADC input channel, maximum input voltage of 1.8V. Reserved, this ADC is used for carrier board version identification. |
| 21 | LED_SYS_STATUS_1V8 | GPIO: typically a 1.8V signal. By default, active-high output to drive Power On LED in the carrier board, which indicates that the running status of software. |
| 95 | MD_LED_PWR_N_1V8 | Active-low output to drive Power On LED in the carrier board, which indicates that the X5 minimum system power-up is complete and reset is released. |

***NOTE:***

1. The state of EMMC_BOOT needs to match the design, otherwise there will be problems such as burning failure and failure to boot.

| EMMC_BOOT Pin Status | System Boot Device |
|---|---|
| NC, keep floating | NAND Flash |
| Pull down to ground through a 4.7K resistor | eMMC |

2. The RDK X5 Module provides two indicator light control interfaces. Both interfaces are only for on-off control and cannot be used as the anode or cathode of an LED for driving or sinking functions.
3. If MD_LED_PWR_N_1V8 is not used to indicate the power-on completion status, leave it floating. It cannot be used for other functions.

## 2.3 Function Interface Circuit Design

### 2.3.1 Ethernet

The RDK X5 module is equipped with a Gigabit Ethernet PHY based on MARVELL's 88E1518 chip solution. This is an Integrated 10/100/1000 Mbps Energy-Efficient Ethernet Transceiver.

The PHY supports the Precise Timing Protocol (PTP) Time Stamping, which is based on IEEE 1588 version 2 and IEEE 802.1AS.

#### 2.3.1.1 Ethernet Interface Design

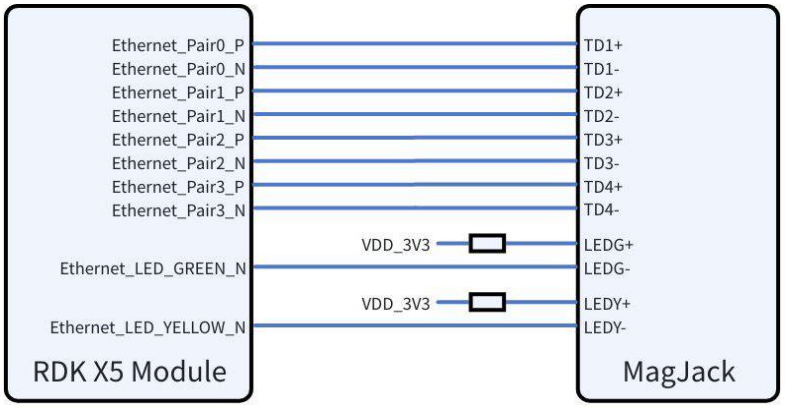
Ethernet interface includes the following pins.

| MD Pin No. | Signal Name | Description |
|---|---|---|
| 3 | Ethernet_Pair3_P | Ethernet pair 3 positive (connect to transformer or MagJack) |
| 4 | Ethernet_Pair1_P | Ethernet pair 1 positive (connect to transformer or MagJack) |
| 5 | Ethernet_Pair3_N | Ethernet pair 3 negative (connect to transformer or MagJack) |
| 6 | Ethernet_Pair1_N | Ethernet pair 1 negative (connect to transformer or MagJack) |
| 9 | Ethernet_Pair2_N | Ethernet pair 2 negative (connect to transformer or MagJack) |
| 10 | Ethernet_Pair0_N | Ethernet pair 0 negative (connect to transformer or MagJack) |
| 11 | Ethernet_Pair2_P | Ethernet pair 2 positive (connect to transformer or MagJack) |
| 12 | Ethernet_Pair0_P | Ethernet pair 0 positive (connect to transformer or MagJack) |
| 15 | Ethernet_LED_GREEN_N | Active-low Ethernet speed indicator, typically a green LED is connected to this pin. |
| 17 | Ethernet_LED_YELLOW_N | Active-low Ethernet speed indicator, typically a yellow LED is connected to this pin |

***NOTE:***

1. The PHY provides two LED control interfaces (Ethernet_LED_GREEN_N and Ethernet_LED_YELLOW_N) for driving the status indicator lights on the MagJack. When the module drives these two signals to a low level, the LED indicator lights will illuminate.

Refer to follow figure for the connecting of MDI interface design.




### 2.3.1.2 Ethernet PCB Design

The following describes the layout recommendations for the MDI differential pairs

- Ensure that the length deviation of each pair of differential signal traces (MDI0+, MDI0−, MDI1+, MDI1−, MDI2+, MDI2−, MDI3+, MDI3−) falls within ±5 mils, and the impedance of the differential trace is 100Ω.

## 2.3.2 USB

The RDK X5 module is equipped with two SoC-integrated USB root ports, specifically a USB 2.0 port and a USB 3.0 port. These ports are directly managed by the SoC's host controller, eliminating the necessity for an intermediate hub conversion.

### 2.3.2.1 USB 2.0 Interface Design

The USB 2.0 port is designed as a Host/Device dual-role interface. It is compliant with the Universal Serial Bus Specification, Revision 2.0, and supports High-Speed (HS), Full-Speed (FS), and Low-Speed (LS) operations.

USB2.0 interface includes the following pins.

| MD Pin No. | Signal Name | Description |
|---|---|---|
| 101 | USB2_ID_3V3 | Input (3.3V signal) USB OTG Pin. Internally pulled up 10K to 3V3. When grounded the Module becomes a USB host but the correct OS driver also needs to be used. |
| 103 | USB2_D_N | USB High-Speed differential transceiver (negative). |
| 105 | USB2_D_P | USB High-Speed differential transceiver (positive). |

***NOTE:***

1. By default, the USB 2.0 port operates in the device mode. In this mode, it enables several key functions, such as firmware flashing, debugging, and virtual network card functionality.
2. Control the USB2_ID_3V3 can change the USB2.0 port role. The relationship between them is shown in the following table. Note that although USB2_ID_3V3 has a default pull-up on the board, the pin is in low state before the system starts up, which does not affect the judgment

of the USB Role during system operation.

| USB2_ID_3V3 STATUS | USB2.0 Role |
|---|---|
| NC | Devices |
| Pull down | Host |

3. When the USB is configured in host mode, the carrier board should have a dedicated power supply to the connector to power the peripherals, and carefully evaluate the problems of overload protection, power backflow, etc. For example: when the board is running and the USB is in host mode, the user incorrectly powers the USB port through the cable.

#### 2.3.2.2 USB 3.0 Interface Design

The USB 3.0 port is designed as a Host/Device dual-role SuperSpeed interface. It adheres to the Universal Serial Bus Specification, Revision 3.0, and supports a wide range of speeds, including Super-Speed (SS), High-Speed (HS), Full-Speed (FS), and Low-Speed (LS).

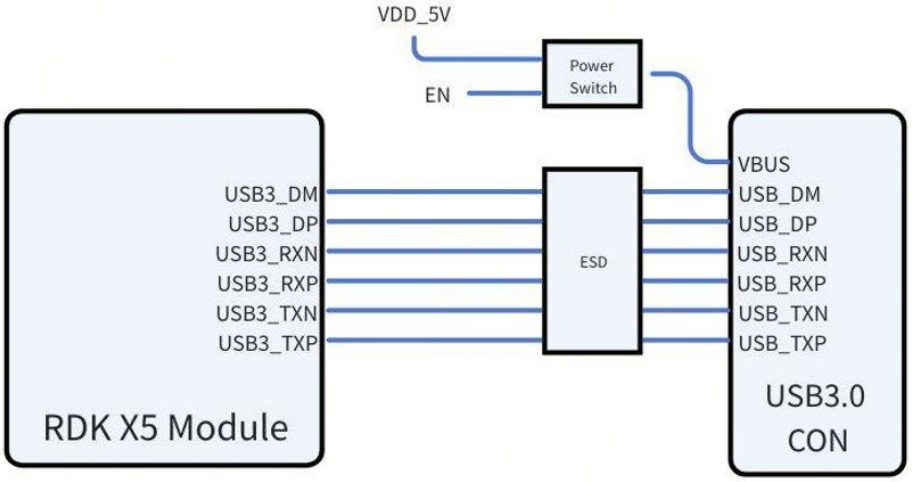
USB3.0 interface includes the following pins.

| MD Pin No. | Signal Name | Description |
|---|---|---|
| 157 | USB3_RXN | USB Super-Speed receiver differential pair (negative). |
| 159 | USB3_RXP | USB Super-Speed receiver differential pair (positive). |
| 163 | USB3_DP | USB High-Speed differential transceiver (positive). |
| 165 | USB3_DM | USB High-Speed differential transceiver (negative). |
| 169 | USB3_TXN | USB Super-Speed transmitter differential pair (negative). |
| 171 | USB3_TXP | USB Super-Speed transmitter differential pair (positive). |

***NOTE:***

1. The 100nF AC coupling capacitors on the super speed signals (USB_TX_P/M and USB_RX_P/M) have already been integrated inside the Module, so the AC coupling capacitors not need added.
2. By default, the USB 3.0 port operates in the device mode, and can be changed to host mode through software configuration.
3. In USB host mode, the board must have an external DCDC or Power Switch to supply 5V power to the USB connector.

Refer to follow figure for the connecting of USB3.0 interface design.




### 2.3.2.3 USB PCB Design

The following describes the layout recommendations for all the USB differential pairs: USB2_D_P, USB2_D_N, USB3_DP, USB3_DM, USB3_TXP, USB3_TXN, USB3_RXP and USB3_RXN.

Must be designed with a differential impedance of 90Ω.

- In order to minimize cross talk, it is recommended that each pair should meet the edge-to-edge 5W principle between differential signal pairs and other signals. Separating with ground as depicted will also help minimize cross talk.
- Route all differential pairs on the same layer adjacent to a solid ground plane.
- Do not route differential pairs over any plane split.
- In addition to the fan-out routing in the USB connector area, it is strongly recommended that the USB routing be on the inner layer and be well grounded.
- Signal vias cannot directly pass through the power plane. It is recommended to use GND to wrap the signal vias when passing through.
- USB routing should avoid the inductor projection area of the switching power supply. If necessary, a magnetically shielded inductor can be selected.
- Adding test points will cause impedance discontinuity and will therefore negatively impact signal performance. If test point are used, they should be placed in series and symmetrically. They must not be placed in a manner that causes stub on the differential pair.
- Avoid 90° turns in trace. The use of bends in differential traces should be kept to a minimum. When bends are used, the number of left and right bends should be as equal as possible and the angle of the bend should be ≥135°. This will minimize any length mismatch causes by the bends and therefore minimize the impact bends have on EMI.
- Minimize the trace lengths of the differential pair traces. The maximum recommended trace length for SuperSpeed differential pair signals and USB 2.0 differential pair signals is eight inches. Longer trace lengths require very careful routing to assure proper signal integrity.
- Match the etch lengths of the differential pair traces. There should be less than 5 mils difference between a SuperSpeed differential pair signal and its complement. The USB 2.0 differential pairs should not exceed 25 mils relative trace length difference.

- The etch lengths of the differential pair groups do not need to match, but all trace lengths should be minimized.

Minimize the use of vias in the differential pair paths as much as possible. If this is not practical, make sure that the same via type and placement are used for both signals in a pair. Any vias used should be placed as close as possible the module.

## 2.3.3 HDMI

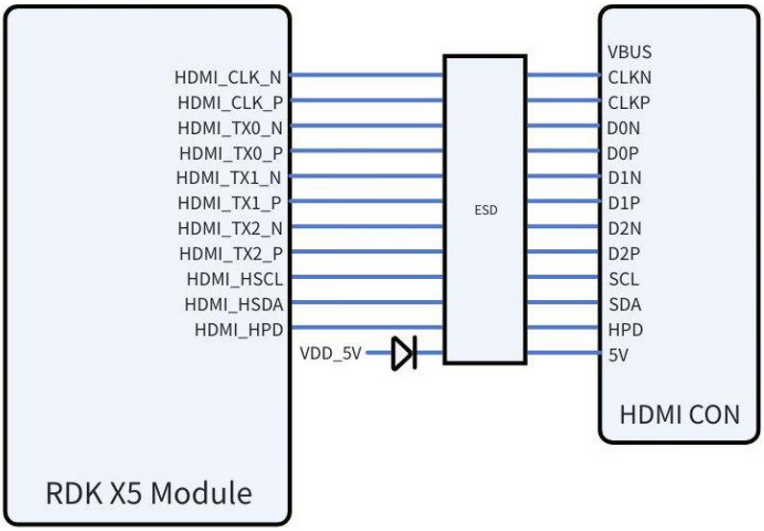
The RDK X5 module provides an HDMI output interface, which supports a resolution of up to 1080P at a frame rate of 60fps.

### 2.3.3.1 HDMI Interface Design

HDMI interface includes the following pins.

| MD Pin No. | Signal Name | Description |
|---|---|---|
| 153 | HDMI_HPD | Input HDMI hot plug. 5V tolerant. It can be connected directly to a HDMI connector, an ESD protection and a 100k pull down resister need to be designed in the carrier board. |
| 170 | HDMI_TX2_P | Output HDMI TX2 positive |
| 172 | HDMI_TX2_N | Output HDMI TX2 negative |
| 176 | HDMI_TX1_P | Output HDMI TX1 positive |
| 178 | HDMI_TX1_N | Output HDMI TX1 negative |
| 182 | HDMI_TX0_P | Output HDMI TX0 positive |
| 184 | HDMI_TX0_N | Output HDMI TX0 negative |
| 188 | HDMI_CLK_P | Output HDMI clock positive |
| 190 | HDMI_CLK_N | Output HDMI clock negative |
| 199 | HDMI_HSDA | Bidirectional HDMI SDA. Internally pulled up with a 2kΩ. 5V tolerant. It can be connected directly to a HDMI connector, an ESD protection need to be designed in the carrier board. |
| 200 | HDMI_HSCL | Bidirectional HDMI SCL. Internally pulled up with a 2kΩ. 5V tolerant. It can be connected directly to a HDMI connector, an ESD protection need to be designed in the carrier board. |

Refer to follow figure for the connecting of HDMI interface design.




### 2.3.3.2 HDMI PCB Design

The following describes the layout recommendations for the HDMI differential pairs

- Ensure that the length deviation of each pair of differential signal traces falls within ±6 mils, and the impedance of the differential trace is 100Ω.
- Control 3 times line width between differential pairs, between differential and other signals
- It is best to make several associated holes at the HDMI signal via to increase the return path.

## 2.3.4 MIPI

RDK X5 module supports for both the MIPI DSI and CSI protocols. In particular, the CSI interface of the RDK X5 module is capable of accommodating up to four independent MIPI links, providing enhanced flexibility and expandability for various applications.

### 2.3.4.1 MIPI DSI TX Interface Design

The module is compatible with the MIPI Alliance Interface specification v1.2, supporting 1 clock lane and up to 4 data lanes, with a maximum data rate of 2.5Gbps per lane.

MIPI DSI interface includes the following pins.

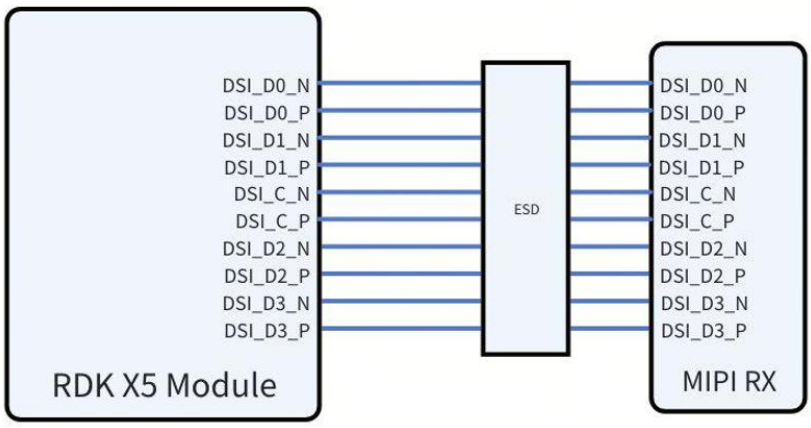
| MD Pin No. | Signal Name | MD Pin No. | Signal Name |
|---|---|---|---|
| 175 | DSI_D0_N | 189 | DSI_C_P |
| 177 | DSI_D0_P | 193 | DSI_D2_N |
| 181 | DSI_D1_N | 194 | DSI_D3_N |
| 183 | DSI_D1_P | 195 | DSI_D2_P |
| 187 | DSI_C_N | 196 | DSI_D3_P |

***NOTE:***

1. When using MIPI DSI TX with 2 lanes, if configured by connecting DSI registers, only lanes 0 and

1can be used, and unused lanes can be NC.

Refer to follow figure for the connecting of MIPI DSI interface design.




### 2.3.4.2 MIPI CSI RX interface

The module is compatible with the MIPI Alliance Interface Specification DPHY V2.1. It supports up to 8 data lanes, with a maximum data rate of 2.5Gbps per lane.

MIPI CSI interface includes the following pins.

| MD Pin No. | Signal Name | MD Pin No. | Signal Name |
|---|---|---|---|
| 127 | CSI0_CLK_N | 140 | CSI2_CLK_N |
| 129 | CSI0_CLK_P | 142 | CSI2_CLK_P |
| 115 | CSI0_D0_N | 128 | CSI2_D0_N |
| 117 | CSI0_D0_P | 130 | CSI2_D0_P |
| 121 | CSI0_D1_N | 134 | CSI2_D1_N |
| 123 | CSI0_D1_P | 136 | CSI2_D1_P |
| 152 | CSI1_CLK_N | 164 | CSI3_CLK_N |
| 154 | CSI1_CLK_P | 166 | CSI3_CLK_P |
| 133 | CSI1_D0_N | 118 | CSI3_D0_N |
| 135 | CSI1_D0_P | 116 | CSI3_D0_P |
| 139 | CSI1_D1_N | 124 | CSI3_D1_N |
| 141 | CSI1_D1_P | 122 | CSI3_D1_P |

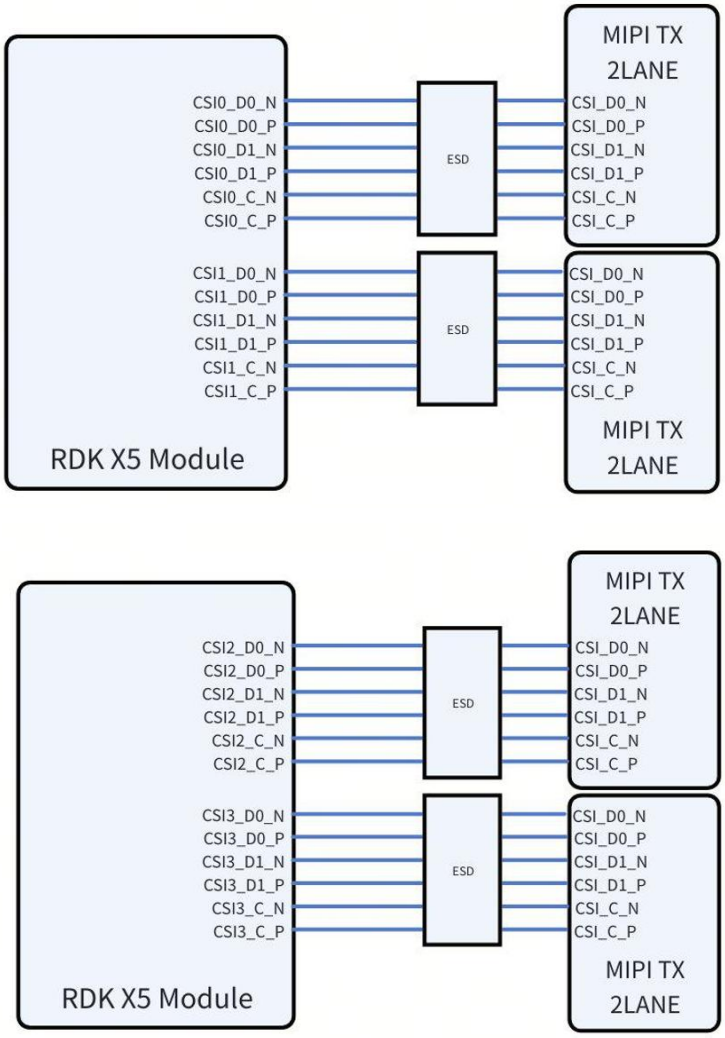
***NOTE:***

1. The CSI interface supports up to 4 MIPI RX links. In this case, each link has an independent differential clock and two data links. Additionally, the CSI interface supports combining 2-lane CSI configurations into a 4-lane CSI application.
2. The RDK X5 Module provides a rich set of GPIO outputs. When working with the default software driver, CAM1_EN_1V8 and CAM2_EN_1V8 are used for the enable and reset control of

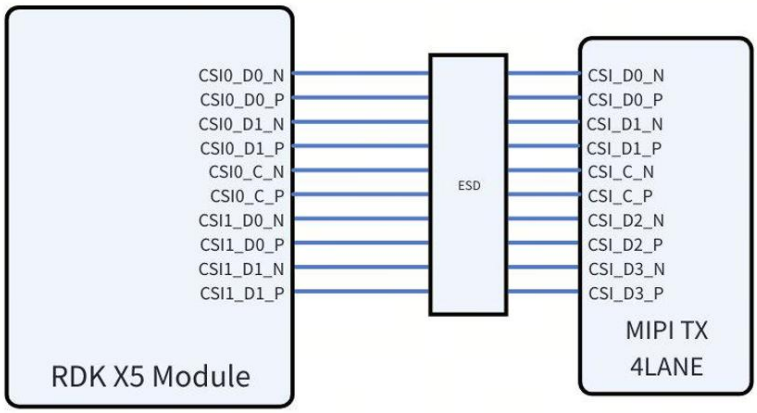
camera modules, adopting 1.8V digital logic. AON_GPIO1_3V3 is employed for the enable control of cameras with 3.3V digital logic.

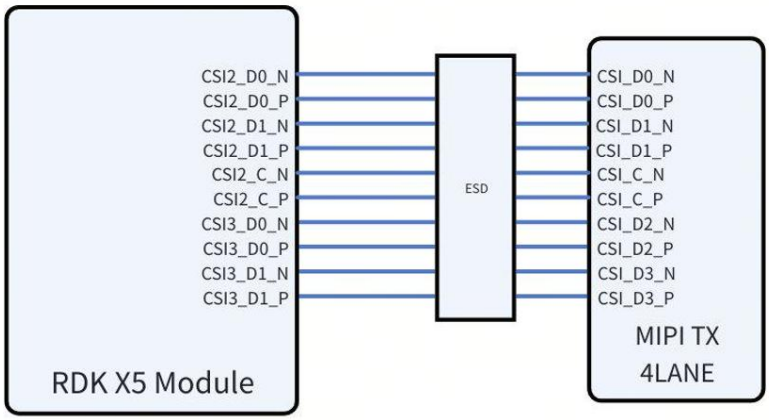
3. For the default configuration of the camera I2C in software, please refer to the I2C section of this document.

The follow figure shows 2-lane mode in which all signals are connected point to point.




The follow figure shows 4-lane mode in which all signals are connected point to point.






### 2.3.4.3 MIPI PCB Design

The routing constraints are shown in the table.

***NOTE:***

**When designing PCB, must import pin delay data on the RDK X5 Module from the Pin Delay sheet of *RDK X5 Module Pinout Description and Application Note. Due to the limitation of board size, MIPI signals are not strictly controlled in equal length on the module.***

| Item | Design Rules |
|---|---|
| Zdiff | 100Ω |
| Routing | ■ The length difference between the signal P\N of the differential pair are within ±1ps<br>■ The delay difference of DATA from CLK are within +/-10ps<br>■ The signal length should be as short as possible.<br>■ MIPI routing should avoid the inductor projection area of the switching power supply. If necessary, a magnetically shielded inductor can be selected. |
| Spacing | ■ The spacing between MIPI traces should meet the edge-to-edge 3W principle, which is applicable to the P/N within a differential pair and between differential pair groups.<br>■ If space permits and there is a reliable ground via design, it is recommended to insert GND traces between differential pair groups and between different CSI interfaces, which will help further reduce EMI and crosstalk between differential pair groups. It should be noted that the spacing between the GND trace and the signal trace should be kept consistent throughout, otherwise it may affect impedance control. |
| External calibration resistors | ■ The routing length from external resistor to X5 CSI_REXT |

| Item | Design Rules |
|---|---|
| | ball should be less than 5mm, and max parasitic capacitance should be less than 2pF.<br>■ The routing length from external resistor to X5 DISP_DPHY_REXT ball should be less than 5mm, and max parasitic capacitance should be less than 2pf. |

## 2.3.5 SD

The RDK X5 Module provides a single SD 3.0 host controller, which utilizes four-wire communication.

- It supports SDR12 at 25 MHz, SDR25 at 50 MHz, SDR50 at 100 MHz, and SDR104 at 200 MHz.
- It is capable of adaptively supporting the two voltage level standards of 3.3V and 1.8V for SD cards.

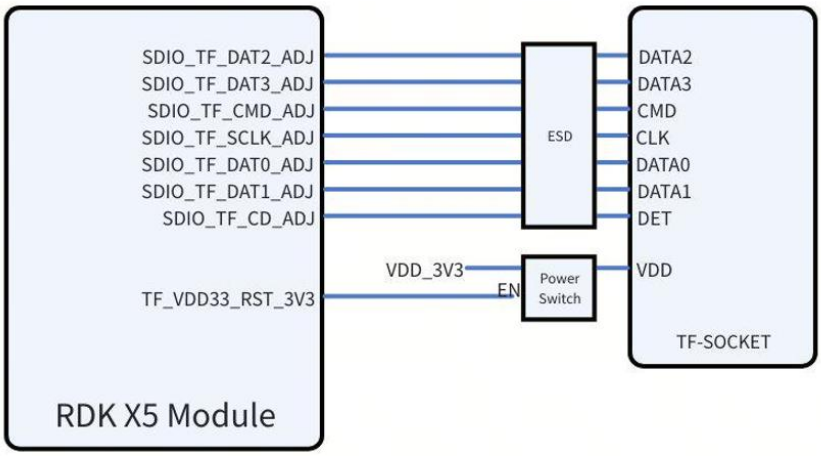
SD interface includes the following pins.

| MD Pin No. | Signal Name | Description |
|---|---|---|
| 57 | SDIO_TF_SCLK_ADJ | SD card clock signal |
| 61 | SDIO_TF_DAT3_ADJ | SD card Data3 signal, internally pulled up 47K to IO power. |
| 62 | SDIO_TF_CMD_ADJ | SD card Command signal, internally pulled up 47K to IO power. |
| 63 | SDIO_TF_DAT0_ADJ | SD card Data0 signal, internally pulled up 47K to IO power. |
| 67 | SDIO_TF_DAT1_ADJ | SD card Data1 signal, internally pulled up 47K to IO power. |
| 69 | SDIO_TF_DAT2_ADJ | SD card Data2 signal, internally pulled up 47K to IO power. |
| 75 | TF_VDD33_RST_3V3 | Output to power-switch for the SD card. The module sets this pin high (3.3V) to signal that power to the SD card should be turned on. |
| 258 | SDIO_TF_CD_ADJ | GPIO: Card Detect signal, internally pulled up 47K to power. When TF inserted, this pin should be high. |

***NOTE:***

- The module offers a control pin named TF_VDD33_RST_3V3 for SD card power supply, which is used to reset the SD card. In the case of using a core module without an on-board EMMC, the SD card will serve as the boot medium. In the design of the carrier board, this control pin must be set to a high level by default. It is recommended to pull it up to 3.3V through a 10k resistor.
- The module provides an SD card insertion detection signal named SDIO_TF_CD_ADJ. When a TF card is inserted, this pin should be at a high level. With default software configuration, a normal close switch type card socket need be selected.

Refer to follow figure for the connecting of SDIO interface design.




#### 2.3.5.1 SD PCB Design

The design requirements on the SDIO signals are as follows:

- Ensure that the spacing between adjacent signal traces complies with the center-to-center 3W rule. Wider spacing between traces helps improve signal quality and reduce crosstalk, especially between CLK signals and other signals.
- Design the trace length of SDIO_TF_DAT [0:3] and SDIO_TF_CMD based on the trace length of SDIO_TF_CLK, and ensure that the deviation falls within ±500 mils.
- The impedance of trace is 50Ω.
- The total trace length cannot exceed 3 inches.

## 2.4 Low Speed Interface

### 2.4.1 I2S

The RDK X5 Module provides two I2S interfaces.

- Two I2S interfaces are full-duplex interfaces and support a maximum data rate of 40 Mbps in master mode.
- In RX mode, it supports 1/2/4/8/16-channel audio input.
- In TX mode, it supports 1/2-channel audio output.

I2S interface includes the following pins.

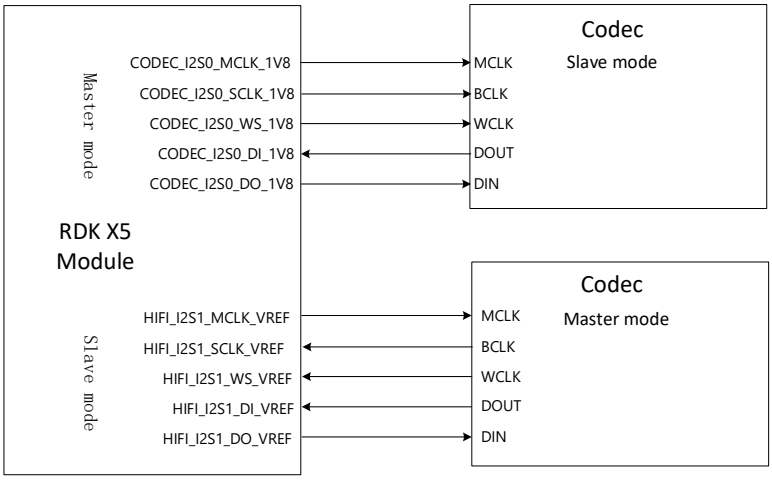
| MD Pin No. | Signal Name | Description |
|---|---|---|
| 236 | CODEC_I2S0_DO_1V8 | GPIO: typically a 1.8V signal, Data Output line for the I2S0 |
| 238 | CODEC_I2S0_SCLK_1V8 | GPIO: typically a 1.8V signal, MCLK signal for the I2S0 |
| 240 | CODEC_I2S0_WS_1V8 | GPIO: typically a 1.8V signal, Word Select signal for the I2S0 |

| | | |
|---|---|---|
| 242 | CODEC_I2S0_DI_1V8 | GPIO: typically a 1.8V signal, Data Input line for the I2S0 |
| 246 | CODEC_I2S0_MCLK_1V8 | GPIO: typically a 1.8V signal, Master Clock (MCLK) signal for the I2S0 |
| **MD Pin No.** | **Signal Name** | **Description** |
| 25 | HIFI_I2S1_DO_VREF | GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V |
| 26 | HIFI_I2S1_WS_VREF | GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V |
| 27 | HIFI_I2S1_DI_VREF | GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V |
| 49 | HIFI_I2S1_SCLK_VREF | GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V |
| 54 | HIFI_I2S1_MCLK_VREF | GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V |

***NOTE:***

1. I2S0 operates with a 1.8V logic level, while I2S1 supports the switching between two voltage levels of 1.8V and 3.3V.

Refer to follow figure for the connecting of I2S interface design.




## 2.4.2 PDM

The RDK X5 Module provides two channel PDM interfaces, which can meet the input requirements of digital microphones.

PDM interface includes the following pins.

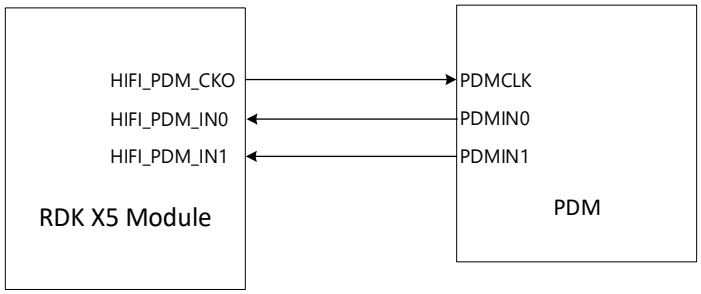
| MD Pin No. | Signal Name | Description |
|---|---|---|
| 21 | LED_SYS_STATUS_1V8 | Pin Function Multiplex:<br>- HIFI_PDM_CKO |

| | | |
|---|---|---|
| 89 | HOST_DIS_WLAN_N_1V8 | Pin Function Multiplex：<br>- HIFI_PDM_IN1 |
| 91 | HOST_DIS_BT_N_1V8 | Pin Function Multiplex：<br>- HIFI_PDM_IN0 |

***NOTE:***

1. On the module, these functions are multiplexed with other GPIO functions and need to be switched through software configuration.

Refer to follow figure for the connecting of PDM interface design.




## 2.4.3 SPI

The RDK X5 Module offers up to four SPI interfaces.

- The SPI interfaces support both master mode and slave mode.
- In master mode, the maximum data rate is 50 Mbps.
- In slave mode, the maximum data rate is 32 Mbps.
- SPI1 supports two chip-select signals.

SPI interface includes the following pins.

| MD Pin No. | Signal Name | Description |
|---|---|---|
| 37 | LSIO_SPI1_SSN0_JTAG_TRSTN_VREF | GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V |
| 38 | LSIO_SPI1_SCLK_JTAG_TCK_VREF | GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V |
| 39 | LSIO_SPI1_SSN1_JTAG_TMS_VREF | GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V |
| 40 | LSIO_SPI1_MISO_JTAG_TDI_VREF | GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V |
| 44 | LSIO_SPI1_MOSI_JTAG_TDO_VREF | GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V |
| **MD Pin No.** | **Signal Name** | **Description** |
| 24 | LSIO_SPI2_MISO_PWM2_VREF | GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V |
| 30 | LSIO_SPI2_CS_PWM1_VREF | GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V |

| | | |
|---|---|---|
| 34 | LSIO_SPI2_SCLK_PWM0_VREF | GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V |
| 45 | LSIO_SPI2_MOSI_PWM3_VREF | GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V |
| **MD Pin No.** | **Signal Name** | **Description** |
| 70 | CAM1_MCLK_1V8 | Pin Function Multiplex:<br>- MCLK<br>- LPWM<br>- SPI3_SCLK |
| 72 | CAM2_MCLK_1V8 | Pin Function Multiplex:<br>- MCLK<br>- LPWM<br>- SPI3_SSN |
| 237 | CAM3_MCLK_1V8 | Pin Function Multiplex:<br>- MCLK<br>- LPWM<br>- SPI3_MISO |
| 239 | CAM4_MCLK_1V8 | Pin Function Multiplex:<br>- MCLK<br>- LPWM<br>- SPI3_MOSI |
| **MD Pin No.** | **Signal Name** | **Description** |
| 203 | CAN_SPI5_MISO | GPIO: Typically a 1.8V signal, SPI5 Master In Slave Out, default for CAN controllers and transceivers in the RDK X5. |
| 204 | CAN_SPI5_CS | GPIO: Typically a 1.8V signal, SPI5 Chip Select, default for CAN controllers and transceivers in the RDK X5. |
| 205 | CAN_SPI5_MOSI | GPIO: Typically a 1.8V signal, SPI5 Master Out Slave In, default for CAN controllers and transceivers in the RDK X5. |
| 206 | CAN_SPI5_SCLK | GPIO: Typically a 1.8V signal, SPI5 Serial Clock, default for CAN controllers and transceivers in the RDK X5. |

#### 2.4.3.1 SPI PCB Design

The design requirements on the SPI signals are as follows:

- Avoid routing signal traces across power plane splits and maintain a complete reference plane for signal traces. If possible, route the SPI on inner layers to avoid EMI emission.
- Ensure that the spacing between adjacent signal traces complies with the center-to-center 2W rule. It is recommended that the distance between the SCLK signal and other signals (including

MISO and MOSI signal) can be 3W or more.

- The signal trace length should be as short as possible.
- If used a low frequency SCLK, SPI signal traces could be set lower priority than other critical signals.

### 2.4.4 I2C

The RDK X5 Module provides 7 I2C interfaces for customized design, while there are total 8 I2C interfaces in X5 chip.

- Only I2C4 supports a data rate of 3.4 Mbps, while I2C0, I2C1, I2C2, I2C3, I2C5, and I2C6 only support up to 400 KHz and the SMBus protocol.
- I2C2 is a dedicated interface for the platform's PMIC and is not used as an interface for peripheral devices.

I2C interface includes the following pins.

| MD Pin No. | Signal Name | Description |
|---|---|---|
| 35 | LSIO_SCL0_PWM4_VREF | GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V. Internal 2kΩ pull up to GPIO_VREF |
| 36 | LSIO_SDA0_PWM5_VREF | GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V. Internal 2kΩ pull up to GPIO_VREF |
| **MD Pin No.** | **Signal Name** | **Description** |
| 28 | LSIO_SDA1_PWM7_VREF | GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V. Internal 2kΩ pull up to GPIO_VREF |
| 31 | LSIO_ SCL1_PWM6_VREF | GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V. Internal 2kΩ pull up to GPIO_VREF |
| **MD Pin No.** | **Signal Name** | **Description** |
| 80 | LSIO_SCL3_3V3 | I2C clock pin, may be used for Camera and Display. Internal 4kΩ pull up to MD_3.3V |
| 82 | LSIO_SDA3_3V3 | I2C Data pin, may be used for Camera and Display. Internal 4kΩ pull up to MD_3.3V |
| **MD Pin No.** | **Signal Name** | **Description** |
| 225 | CAM2_SDA4_1V8 | GPIO: typically a 1.8V signal, Camera2 Serial Data Line in RDK X5, no pull up resisters in the module. |
| 227 | CAM2_SCL4_1V8 | GPIO: typically a 1.8V signal, Camera2 Serial Clock Line in RDK X5, no pull up resisters in the module. |
| **MD Pin No.** | **Signal Name** | **Description** |

| | | |
|---|---|---|
| 56 | LSIO_SCL5_RX3_VREF | GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V. Internal 4kΩ pull up to GPIO_VREF |
| 58 | LSIO_SDA5_TX3_VREF | GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V. Internal 4kΩ pull up to GPIO_VREF |
| **MD Pin No.** | **Signal Name** | **Description** |
| 241 | CAM1_SDA6_1V8 | GPIO: typically a 1.8V signal, Camera1 Serial Data Line in RDK X5, no pull up resisters in the module. |
| 243 | CAM1_SCL6_1V8 | GPIO: typically a 1.8V signal, Camera1 Serial Clock Line in RDK X5, no pull up resisters in the module. |
| **MD Pin No.** | **Signal Name** | **Description** |
| 209 | CODEC_HDMI_SCL7 | GPIO: Typically a 1.8V signal, Serial Clock Line, the clock signal for the I2C bus. By default, it is used as I2C for codec (located on the carrier board) and HDMI converter chip (located on the module) in the RDK X5. Internal 2kΩ pull up to 1.8V. |
| 211 | CODEC_HDMI_SDA7 | GPIO: Typically a 1.8V signal, Serial Data Line, the data line for the I2C bus. By default, it is used as I2C for codec (located on the carrier board) and HDMI converter chip (located on the module) in the RDK X5. Internal 2kΩ pull up to 1.8V. |

***NOTE:***

1. With the default software driver, I2C2 and I2C6 are utilized as the I2C control buses for two cameras, employing 1.8V digital logic. I2C3 serves as the camera I2C bus with 3.3V digital logic.

## 2.4.5 UART

The RDK X5 Module provides 6 UART interfaces for customized design, while there are total 8 UART interfaces in X5 chip.

- UART0 is a dedicated interface for system debugging and operates at a frequency of 921600 bps.
- UART5 is used for the onboard Bluetooth and WiFi modules and cannot be used for other peripherals.
- UART2, UART3, UART4, UART5, UART6, and UART7 support baud rates of 9600, 38400, 57600, 921600, 115200, and 4M.
- UART2, UART3, UART4, UART5, and UART6 support the standard mode.
- UART7 supports the auto-flow control mode.

UART interface includes the following pins.

| MD Pin No. | Signal Name | Description |
|---|---|---|
| 64 | DEBUG_UART0_TXD_1V8 | Uart Data TX pin, a 1.8V signal, used to debug X5 chip |

| | | |
|---|---|---|
| 68 | DEBUG_UART0_RXD_1V8 | Uart Data RX pin, a 1.8V signal, used to debug X5 chip |
| **MD Pin No.** | **Signal Name** | **Description** |
| 51 | LSIO_UART1_RX_VREF | GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V |
| 55 | LSIO_UART1_TX_VREF | GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V |
| **MD Pin No.** | **Signal Name** | **Description** |
| 41 | LSIO_UART2_RX_VREF | GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V |
| 46 | LSIO_UART2_TX_VREF | GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V |
| **MD Pin No.** | **Signal Name** | **Description** |
| 56 | LSIO_SCL5_RX3_VREF | GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V. Internal 1.8kΩ pull up to GPIO_VREF |
| 58 | LSIO_SDA5_TX3_VREF | GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V. Internal 1.8kΩ pull up to GPIO_VREF |
| **MD Pin No.** | **Signal Name** | **Description** |
| 215 | UART4_RXD | GPIO: Receive Data line for UART4, typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V |
| 217 | UART4_TXD | GPIO: Transmit Data line for UART4, typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V |
| **MD Pin No.** | **Signal Name** | **Description** |
| 29 | LSIO_UART7_CTS_N_VREF | Pin Function Multiplex：UART6_RX |
| 47 | LSIO_UART7_RTS_N_VREF | Pin Function Multiplex：UART6_TX |
| **MD Pin No.** | **Signal Name** | **Description** |
| 29 | LSIO_UART7_CTS_N_VREF | GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V |
| 47 | LSIO_UART7_RTS_N_VREF | GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V |
| 48 | LSIO_UART7_RX_VREF | GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V |
| 50 | LSIO_UART7_TX_VREF | GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V |

***NOTE:***

1. The Pin names of the UART module (TX&RX) are from the view of X5. For example, UART1_TXD is a transmitting signal and output from X5, meanwhile UART1_RXD is a receiving signal and input to X5.
2. If DEBUG_UART0 (Pin64, Pin68) need to be pulled up, the pull-up power supply must to use VDDIO18_DSP_UART (Pin231).

## 2.4.6 PWM

The RDK X5 Module supports 8 PWM interfaces.

- The frequency of the output waveform is programmable, ranging from 0.05 Hz to 1MHz.
- It also provides a reference mode and can output waveforms with various duty cycles.

| MD Pin No. | Signal Name | Description |
|---|---|---|
| 34 | LSIO_SPI2_SCLK_PWM0_VREF | GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V |
| 30 | LSIO_SPI2_CS_PWM1_VREF | GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V |
| 24 | LSIO_SPI2_MISO_PWM2_VREF | GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V |
| 45 | LSIO_SPI2_MOSI_PWM3_VREF | GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V |
| 35 | LSIO_SCL0_PWM4_VREF | GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V. Internal 2kΩ pull up to GPIO_VREF |
| 36 | LSIO_SDA0_PWM5_VREF | GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V. Internal 2kΩ pull up to GPIO_VREF |
| 31 | LSIO_ SCL1_PWM6_VREF | GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V. Internal 2kΩ pull up to GPIO_VREF |
| 28 | LSIO_SDA1_PWM7_VREF | GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V. Internal 2kΩ pull up to GPIO_VREF |

### 2.4.6.1 PWM PCB Design

The design requirements on the PWM signals are as follows:

- For high frequency PWM design, avoid routing signal traces across power plane splits and maintain a complete reference plane for signal traces. Ensure that the spacing between adjacent signal traces complies with the center-to-center 2W rule.

## 2.4.7 LPWM

RDK X5 Module provides a total of 8 channels of LPWM.

- The frequency of the output pulse is programmable, ranging from 1 Hz to 1 MHz.
- The width of the output pulse is programmable, ranging from 1 μs to 4 ms.
- It supports generating output pulses with multiple trigger sources, such as PPS, EMAC, and the internal system timer.

| MD Pin No. | Signal Name | Description |
|---|---|---|
| 206 | CAN_SPI5_SCLK | Pin Function Multiplex：LPWM0 |
| 204 | CAN_SPI5_CS | Pin Function Multiplex：LPWM1 |
| 203 | CAN_SPI5_MISO | Pin Function Multiplex：LPWM2 |
| 205 | CAN_SPI5_MOSI | Pin Function Multiplex：LPWM3 |
| 70 | CAM1_MCLK_1V8 | Pin Function Multiplex：LPWM4 |
| 72 | CAM2_MCLK_1V8 | Pin Function Multiplex：LPWM5 |
| 237 | CAM3_MCLK_1V8 | Pin Function Multiplex：LPWM6 |
| 239 | CAM4_MCLK_1V8 | Pin Function Multiplex：LPWM7 |

***NOTE:***

1. The four channels of signals (Pin 70, Pin 72, Pin 237, Pin 239) are based on the same clock source. Therefore, when used for LPWM synchronization, they can be directly connected one-to-one without the need for a one-to-many connection method.
2. The four channels of signals (Pin 203, Pin 204, Pin 205, Pin 206) are based on the same clock source.

### 2.4.7.1 LPWM PCB Design

The design requirements on the LPWM signals are as follows:

- For high frequency LPWM design, avoid routing signal traces across power plane splits and maintain a complete reference plane for signal traces. Ensure that the spacing between adjacent signal traces complies with the center-to-center 2W rule.

## 2.4.8 MCLK

The RDK X5 Module provides four channels of MCLK signals, which can be used to drive the camera module.

| MD Pin No. | Signal Name | Description |
|---|---|---|
| 70 | CAM1_MCLK_1V8 | Pin Function Multiplex：LPWM4 |
| 72 | CAM2_MCLK_1V8 | Pin Function Multiplex：LPWM5 |
| 237 | CAM3_MCLK_1V8 | Pin Function Multiplex：LPWM6 |
| 239 | CAM4_MCLK_1V8 | Pin Function Multiplex：LPWM7 |

## 2.4.9 ADC

The RDK X5 Module has 4 ADCs.

- ADC7 is used for the hardware identification of the carrier board, which facilitates customers to distinguish the board ID.
- The other 3 ADCs can be used for various types of data collection and voltage monitoring.

| MD Pin No. | Signal Name | Description |
|---|---|---|
| 210 | ADC_VINS4 | The 4th ADC input channel, maximum input voltage of 1.8V |
| 212 | ADC_VINS3 | The 3rd ADC input channel, maximum input voltage of 1.8V |
| 216 | ADC_VINS7_RSVD | The 7th ADC input channel, maximum input voltage of 1.8V. |
| 218 | ADC_VINS5 | The 5th ADC input channel, maximum input voltage of 1.8V |

***NOTE***:

1. In practical applications, it is recommended that the ADC's sampling voltage range be maintained between approximately 100mV and 1700mV, as this helps improve the sampling accuracy of the ADC. Additionally, configuring an appropriate operating mode and sampling rate through software can help achieve a balance between accuracy and resource utilization.

## 2.4.10 AON GPIO

The RDK X5 Module supports the sleep mode. The following three GPIOs can wake up the X5 in sleep mode.

- AON_FLASH_SLEEP_RESUME_N_1V8 is fixedly used for the sleep/wake-up function in the software.
- AON_GPIO0 and AON_GPIO4 has a 10k pull-up resistor design, and the pull-up voltage level is 1.8V on the module and can be further developed on the baseboard according to requirements.
- When using the sleep wakeup function, if the X5 chip is in sleep mode, the peripherals need to be powered to ensure that the peripherals can generate valid interrupt signals.

| MD Pin No. | Signal Name | Description |
|---|---|---|
| 222 | AON_GPIO4 | GPIO: typically a 1.8V signal, can be used for interrupt wakeup in sleep mode |
| 248 | AON_GPIO0 | GPIO: typically a 1.8V signal, can be used for interrupt wakeup in sleep mode |
| 93 | AON_FLASH_SLEEP_RESUME_N_1V8 | Low level on this pin realizes different function. This pin is not connected to any net on the module. By pulling it low, the X5 minimum system can be switched between sleep and wake-up states. Pull it low during the system startup phase to perform the burning operation. |

## 2.5 PIN Delay

D-Robotics recommends that customers control the delay of high-speed signals and pay attention to the impact of PCB material and routing form on signal speed during the process. The Pin Delay sheet of ***RDK X5 Module Pinout Description and Application Note*** shows the pin delay data on the RDK X5 Module.

***NOTE:***

**When routing *MIPI CSI signals*, must import the pin delay data. *Due to the limitation of board size, MIPI CSI signals are not strictly controlled in equal length on the module.***

## 2.6 Wireless Cutout

The RDK X5 module supports onboard WiFi antenna modules, so in the carrier board design, clearance design should be done at the corresponding projection position.